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*Jokanovic, D.; Yamano, K.; Ohta, M.; Shiratori, N.;*  
 TENCON '92. Technology Enabling Tomorrow : Computers, Communications & Automation towards the 21st Century. 1992 IEEE Region 10 International Conference. , 11-13 Nov. 1992  
 Pages:212 - 216 vol.1

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2 **Efficient memory integrity verification and encryption for secure processors**

*Suh, G.E.; Clarke, D.; Gasend, B.; van Dijk, M.; Devadas, S.;*  
 Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM International Symposium on , 3-5 Dec. 2003  
 Pages:339 - 350

[\[Abstract\]](#)    [\[PDF Full-Text \(431 KB\)\]](#)    **IEEE CNF**
3 **A Compact model for analysis and design of on-chip power network decoupling capacitors**

*Zarkesh-Ha, P.; Doniger, K.; Loh, W.; Sun, D.; Stephani, R.; Priebe, G.;*  
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*Onufryk, P.Z.;*  
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**5 Facilitating program verification with dependent types**

*Hongwei Xi;*

Software Engineering and Formal Methods, 2003.Proceedings. First Internatic  
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2003. HPCA-9 2003. Proceedings. , 8-12 Feb. 2003  
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**8 Combining ATPG and symbolic simulation for efficient validation of embedded array systems**

*Parthasarathy, G.; Iyer, M.K.; Tao Feng; Wang, L.-C.; Kwang-Ting Cheng; Al  
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**10 Using a hardware model checker to verify software**

*Edwards, S.A.; Ma, T.; Damiano, R.;*

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**11 Schedulability analysis of acyclic processes**

*Meyer, M.J.; Wong-Toi, H.;*

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12 **System chip test: are we there yet?**

*Varma, P.;*

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13 **Micro/miniature shape memory alloy actuator**

*Ikuta, K.;*

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